MMDF3N06VL

Power MOSFET
3 Amps, 60 Volts
N−Channel SO−8, Dual

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

Features

- On−resistance Area Product about One−half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E−FET™ Predecessors
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E−FET
- Miniature SO−8 Surface Mount Package − Saves Board Space
- Mounting Information for SO−8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	60	Vdc
Drain−to−Gate Voltage, (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	± 15	Vdc
Drain Current − Continuous @ T_A = 25°C − Continuous @ T_A = 100°C − Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	3.3 0.7 10	Adc Apk
Total Power Dissipation @ T_A = 25°C (Note 1)	P_D	2.0	W
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 3.3 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	54	mJ
Thermal Resistance, Junction to Ambient (Note 1)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 0.0625″ from case for 10 seconds	T_L	260	°C

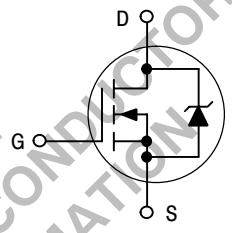
1 Mounted on G10/FR4 glass epoxy board using minimum recommended footprint.

ON Semiconductor®

http://onsemi.com

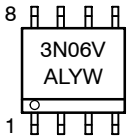
V_{DSS}	$R_{DS(ON)}$ TYP	I_D MAX
60 V	130 mΩ	3.0 A

N−Channel



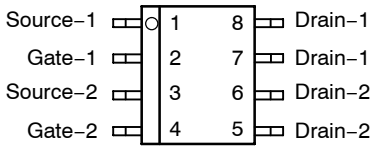
SO−8
CASE 751
STYLE 11

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN ASSIGNMENT



Top View

ORDERING INFORMATION

Device	Package	Shipping†
MMDF3N06VLR2	SO−8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

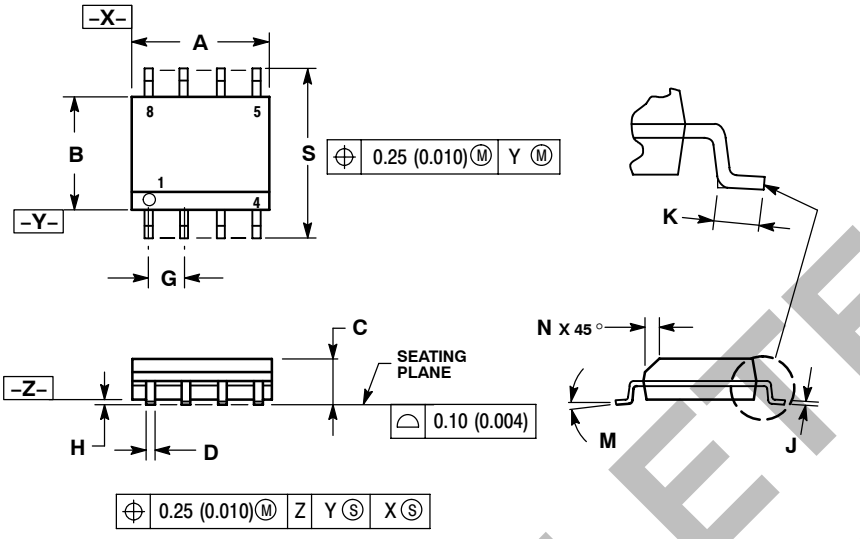
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 –	 – 66	 – –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	 – –	 – –	 10 100	μAdc
Gate−Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	100	nAdc
ON CHARACTERISTICS (Note 1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 –	 1.5 3.0	 2.0 –	Vdc mV/°C
Static Drain−to−Source On−Resistance (V_{GS} = 5.0 Vdc, I_D = 3.3 Adc)		$R_{DS(on)}$	–	0.12	0.13	Ω
Drain−to−Source On−Voltage (V_{GS} = 5.0 Vdc, I_D = 3.3 Adc) (V_{GS} = 5.0 Vdc, I_D = 1.65 Adc, T_J = 150°C)		$V_{DS(on)}$	 – –	 – –	 0.5 0.4	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.65 Adc)		g_{FS}	1.0	3.0	–	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	340	480	pF
Output Capacitance		C_{oss}	–	110	150	
Transfer Capacitance		C_{rss}	–	27	50	
SWITCHING CHARACTERISTICS (Note 2)						
Turn−On Delay Time	(V_{DD} = 30 Vdc, I_D = 3.3 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	–	10	20	ns
Rise Time		t_r	–	30	60	
Turn−Off Delay Time		$t_{d(off)}$	–	32	60	
Fall Time		t_f	–	28	60	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 3.3 Adc, V_{GS} = 5.0 Vdc)	Q_T	–	9.0	20	nC
		Q_1	–	1.5	–	
		Q_2	–	4.3	–	
		Q_3	–	3.5	–	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage (Note 1)	(I_S = 3.3 Adc, V_{GS} = 0 Vdc) (I_S = 3.3 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	 – –	 0.84 0.67	 1.2 –	Vdc
Reverse Recovery Time	(I_S = 3.3 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	–	58	–	ns
		t_a	–	38	–	
		t_b	–	20	–	
Reverse Recovery Storage Charge		Q_{RR}	–	0.11	–	μC

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS

SO−8
CASE 751−07
ISSUE AB

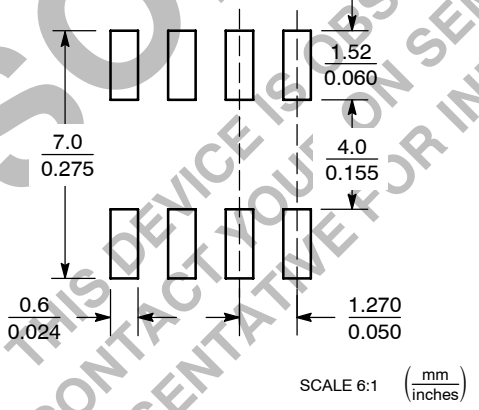


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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